I CLAIM:

1. A high side current monitor circuit, comprising:

a high side terminal;

a load side terminal;

a current sensing element connected between said high and load side terminals which carries a current of interest I_{sense} and which develops a shunt voltage V_{sense} between said high side and load side terminals in response to I_{sense}, said shunt voltage having a common mode voltage V_{cm} with respect to a ground terminal;

an operational amplifier, said amplifier's non-inverting input coupled to said load side terminal;

a first resistor connected between said high side terminal and said amplifier's inverting input;

a first transistor having a control input and a current circuit, said control input connected to the output of said amplifier and said current circuit connected between said inverting input and a current output node such that said first transistor conducts an output current I_{out} through said first resistor to said current output node necessary to make the voltages at said inverting and non-inverting inputs equal such that I_{out} is proportional to I_{sense};

an output load resistor connected between a second node and said ground terminal; and

a second transistor coupled between said current output node and said second node and connected to conduct said output current to said load resistor such that a voltage proportional to I_{sense} and referred to said ground terminal is developed at said second node.

2. The current monitor circuit of claim 1, wherein

said amplifier, first resistor and first transistor comprise an integrated circuit (IC) having an associated process breakdown voltage, said second transistor and said output load resistor standing off a substantial portion of said common mode voltage such that the common mode voltage to which said IC is subjected is less than said process breakdown voltage.

3. The current monitor circuit of claim 2, wherein said amplifier is operated with an operating voltage referred to a common terminal and said second transistor is a P-type field-effect transistor (PFET) having its source connected to said current output node, its drain connected to said second node, and its gate connected to said common terminal.

4. The current monitor circuit of claim 2, wherein said second transistor is a PNP bipolar transistor having its emitter connected to said current output node and its collector connected to said second node, said current monitor circuit further comprising a base current recycling circuit arranged to cause the current in said first resistor to be incremented by an amount approximately equal to said second transistor's base current.

5. The current monitor circuit of claim 4, wherein said base current recycling circuit comprises:

a third resistor interposed between said load side terminal and said amplifier's non-inverting input and having a resistance approximately equal to that of said first resistor; and

a current mirror connected to the base of said second transistor and to said amplifier's non-inverting input such that said second transistor's base current is mirrored to said amplifier's non-inverting input and said

mirrored current flows through said third resistor, such that said amplifier increments the current in said first resistor and thereby in I_{out} by an amount approximately equal to said base current to equalize the voltages at its inverting and non-inverting inputs.

6. The current monitor circuit of claim 1, further comprising a voltage limiter coupled between said high side terminal and said common terminal which establishes an operating voltage for said amplifier and enables said amplifier to be powered from a voltage lower than V_{cm}.

7. The current monitor circuit of claim 6, further comprising a bias current source coupled to said common terminal which provides an operating current for said amplifier.

8. The current monitor circuit of claim 7, wherein said bias current source comprises a resistor connected between said common terminal and said ground terminal.

9. The current monitor circuit of claim 7, wherein said bias current source is a bias circuit comprising:

a first PNP transistor having its emitter coupled to said common terminal;

a second PNP transistor having its emitter connected to the emitter of said first PNP transistor, and its base and collector connected to the base of said first PNP transistor;

a second resistor connected between the common bases and common emitters of said first and second PNP transistors;

a first NPN transistor having its emitter connected to a bias terminal, said first NPN transistor diode-connected;

a second NPN transistor having its base connected to the base of said first NPN transistor;

a third resistor connected between the emitters of said first and second NPN transistors;

a fourth resistor connected between the base of said second PNP transistor and the collector of said first NPN transistor; and

a third PNP transistor having its emitter connected to the collector of said second PNP transistor, its collector connected to the collector of said first NPN transistor, and its base connected to the collector of said second NPN transistor;,

the emitter of said second NPN transistor being larger than the emitter of said first NPN transistor.

10. The current monitor circuit of claim 9, wherein said bias terminal is connected to said ground terminal such that said bias circuit provides said bias current to said common terminal.

11. The current monitor circuit of 6, wherein said voltage limiter comprises a zener diode.

12. The current monitor circuit of 6, wherein said voltage limiter comprises an avalanche breakdown diode.

13. The current monitor circuit of 6, wherein said voltage limiter comprises a bandgap shunt regulator.

14. A dual-use integrated circuit (IC) high side current monitor circuit suitable for use in measuring currents of interest having common mode voltages either above or below a predetermined process breakdown voltage, said IC comprising:

a high side terminal;

a load side terminal, said high and load side terminals suitable for connection across a current sensing element which carries a current of interest I_{sense} and which develops a shunt voltage V_{sense} between said high side and load side terminals in response to I_{sense}, said shunt voltage having a common mode voltage V_{cm} with respect to an external ground terminal;

an operational amplifier operated with an operating voltage referred to an IC common terminal, said amplifier having an associated breakdown voltage;

a first resistor connected between said high side terminal and said amplifier's inverting input;

a second resistor connected between said load side terminal and said amplifier's non-inverting input, said second resistor having a resistance approximately equal to that of said first resistor;

a first transistor having a control input and a current circuit, said control input connected to the output of said amplifier and said current circuit connected between said inverting input and a current output terminal such that said first transistor conducts an output current I_{out} through said first resistor to said current output terminal necessary to make the voltages at said inverting and non-inverting inputs equal such that I_{out} is proportional to I_{sense};

a base current recycling circuit comprising an alpha terminal and arranged to cause the current in said first resistor to be incremented by an amount approximately equal to a current conducted at said alpha terminal;

a voltage limiter coupled between said high side terminal and said IC common terminal which establishes an operating voltage and provides operating current for said amplifier, said operating current varying with a bias current applied to said IC at said common terminal; and

a bias circuit coupled between said common

terminal and a bias terminal and arranged to provide said bias current to said common terminal when enabled.

15. The dual-use IC of claim 14, further comprising:

an output load resistor external to said IC connected between a second node and said external ground terminal; and

a second transistor external to said IC coupled between said current output terminal and said second node and connected to conduct said output current to said load resistor such that a ground-referred voltage proportional to I_{sense} is developed at said second node,

said second transistor and said output load resistor standing off a substantial portion of said common mode voltage such that the common mode voltage to which said IC is subjected is less than said process breakdown voltage.

16. The dual-use IC of claim 15, wherein said second transistor is a P-type field-effect transistor (PFET) having its source connected to said current output node, its drain connected to said second node, and its gate connected to said IC common terminal.

17. The dual-use IC of claim 15, wherein said second transistor is a PNP bipolar transistor having its emitter connected to said current output node, its collector connected to said second node, and its base connected to said alpha terminal, such that the current in said first resistor is incremented by an amount approximately equal to said second transistor's base current.

18. The dual-use IC of claim 15, wherein said base current recycling circuit comprises a current mirror connected to an "alpha" terminal and to said amplifier's

non-inverting input such that a current conducted at said alpha terminal is mirrored to said amplifier's non-inverting input and said mirrored current flows through said second resistor, such that said amplifier increments the current in said first resistor by an amount approximately equal to said current conducted at said alpha terminal.

19. The dual-use IC of claim 14, wherein said bias circuit comprises:

a first PNP transistor having its emitter coupled to said common terminal;

a second PNP transistor having its emitter connected to the emitter of said first PNP transistor, and its base and collector connected to the base of said first PNP transistor;

a third resistor connected between the common bases and common emitters of said first and second PNP transistors;

a first NPN transistor having its emitter connected to said bias terminal, said first NPN transistor diode-connected;

a second NPN transistor having its base connected to the base of said first NPN transistor;

a fourth resistor connected between the emitters of said first and second NPN transistors;

a fifth resistor connected between the base of said second PNP transistor and the collector of said first NPN transistor; and

a third PNP transistor having its emitter connected to the collector of said second PNP transistor, its collector connected to the collector of said first NPN transistor, and its base connected to the collector of said second NPN transistor;,

the emitter of said second NPN transistor being

larger than the emitter of said first NPN transistor.

20. The dual-use IC of claim 19, wherein said bias terminal is connected to said ground terminal such that said bias circuit is enabled and provides said bias current to said common terminal.

21. The dual-use IC of claim 19, wherein said bias terminal is connected to said common terminal such that said bias circuit is disabled, further comprising a resistor connected between said bias and common terminals and said ground terminal such that said resistor provides said bias current to said common terminal.

22. The dual-use IC of claim 19, further comprising:

an output load resistor external to said IC connected between a second node and said external ground terminal; and

a second transistor external to said IC coupled between said current output terminal and said second node and connected to conduct said output current to said load resistor such that a ground-referred voltage proportional to I_{sense} is developed at said second node,

said second transistor and said output load resistor standing off a substantial portion of said common mode voltage such that the common mode voltage to which said IC is subjected is less than said process breakdown voltage;

said bias terminal connected to said common terminal such that said bias circuit is disabled, further comprising a resistor connected between said bias and common terminals and said ground terminal such that said resistor provides said bias current to said common terminal.

23. The dual-use IC of claim 19, further comprising an output load resistor external to said IC connected between said current output terminal and said external ground terminal such that a ground-referred voltage proportional to I_{sense} is developed at said current output terminal, said bias terminal connected to said ground terminal such that said bias circuit is enabled and provides said bias current to said common terminal.

24. The dual-use IC of claim 14, further comprising an output load resistor external to said IC connected between said current output terminal and said external ground terminal such that a ground-referred voltage proportional to I_{sense} is developed at said current output terminal.

25. The dual-use IC of claim 14, wherein said voltage limiter comprises a zener diode.

26. The dual-use IC of claim 14, wherein said voltage limiter comprises an avalanche breakdown diode.

27. The dual-use IC of claim 14, wherein said voltage limiter comprises a bandgap shunt regulator.